What is claimed is:

1. A semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type formed in a surface layer portion on a principal surface in a semiconductor substrate of a first conductivity type, the source region being formed to be shallower than the base region in the surface layer portion on the principal surface in the base region;

a drain region of the first conductivity type formed in a position apart from the base region in the surface layer portion on the principal surface;

a well region of the first conductivity type disposed in the surface layer portion on the p rincipal surface and formed to be deeper than the drain region and to have a higher concentration than the semiconductor substrate in a region including the drain region and in contact with the base region ;

a trench formed in the principal surface of the semiconductor substrate to penetrate the base region in a direction toward the drain region from the source region as a planar structure thereof;

a gate electrode formed via a gate insulating film in the inside of the trench;

a source electrode electrically connected to the source region; and

a drain electrode electrically connected to the drain region.

2. A semiconductor device according to claim 1, wherein the concentration of the well region increases continuously from a bottom to a surface.

3. A semiconductor device according to claim 1, wherein, at least in the surface layer portion on the principal surface in the base region, a base contact region of the second conductivity type is shallower and has a higher concentration than the base region and is formed between the source region and the drain region.

4. A semiconductor device according to claim 3, wherein the base contact region is formed apart from the trench, and a gate electrode is formed on the principal surface via a gate insulating film.

5. A semiconductor device according to claim 4, further comprising:

an embedded layer of the first conductivity type having a higher concentration than the semiconductor substrate formed in a lower portion of the semiconductor substrate, wherein a bottom surface corner portion of the trench is deeper than the well region and shallower than the embedded layer.

6. A semiconductor device according to claim 1, further comprising:

an embedded layer of the first conductivity type having

a higher concentration than the semiconductor substrate formed in a lower portion of the semiconductor substrate, wherein a bottom surface corner portion of the trench is deeper than the well region and shallower than the embedded layer.

7. A semiconductor device according claim 1, further comprising another gate electrode arranged in an opening of the source region on a side of the trench.

8. A semiconductor device according to claim 1, wherein the semiconductor substrate comprises an SOI substrate, and the trench is formed to reach an embedded insulating film of the SOI substrate.

9. A semiconductor device according to claim 1, wherein the semiconductor substrate comprises an SOI substrate, and a thickness of a semiconductor layer on an embedded insulating film in the SOI substrate is substantially equal to a depth of the well region.

10. A semiconductor device according to claim 1, wherein the drain region and the well region form an island shape, and the base region exists around the drain and well regions.

11. A semiconductor device according to claim 1, further comprising a source cell and a drain cell arranged alternately lengthwise and crosswise adjacent to each other.

12. A semiconductor device according to claim 1, further comprising at least a source contact in an outermost circumference in a group of cells provided in parallel adjacent to each other and that is set larger in size than inner source contacts.

13. A semiconductor device according to claim 1, further comprising a base contact region of a second conductivity type having a higher concentration than the base region, wherein the base contact region is formed in at least the surface layer portion on the principal surface in the base region in a position where at least the source region in an outermost circumference in a group of cells provided in parallel adjacent to each other is arranged.

14. A semiconductor device according to claim 13, wherein the drain region is surrounded by the source region and the base contact region as a planar structure.

15. A method of manufacturing the semiconductor device of claim 1, the method comprising:

arranging an insulating film on the principal surface in which a region where a base contact is to be formed is opened as a contact hole, after forming the base region, the source region, the drain region, the well region, and the trench; and

performing ion implantation using the insulating film

as a mask to form a base contact region apart from the trench in the surface layer portion on the principal surface.

16. A semiconductor device comprising:

an emitter region of a first conductivity type;

a base region of a second conductivity type formed in a surface layer portion on a principal surface in a semiconductor substrate of a first conductivity type, the emitter region of the first conductivity type being formed to be shallower than the base region in the surface layer portion on the principal surface in the base region;

a collector region of the second conductivity type formed in a position apart from the base region in the surface layer portion on the principal surface;

a well region of the first conductivity type disposed in the surface layer portion on the principal surface, the well region is formed to be deeper than the collector region and to have a higher concentration than the semiconductor substrate in a region including the collector region and to be in contact with the base region;

a trench formed in the principal surface of the semiconductor substrate to penetrate the base region in a direction toward the collector region from the emitter region as a planar structure thereof;

a gate electrode which is formed via a gate insulating film in the inside of the trench ;

an emitter electrode which is electrically connected to

the emitter region; and

a collector electrode which is electrically connected to the collector region.

17. A method of manufacturing the semiconductor device of claim 16, the method comprising:

arranging an insulating film in which a region where a base contact is to be formed is opened as a contact hole on the principal surface after forming the base region, the emitter region, the collector region, the well region, and the trench; and

performing ion implantation using the insulating film as a mask to form a base contact region apart from the trench in the surface layer portion on the principal surface.

18. A semiconductor device according to claim 16, wherein, at least in the surface layer portion on the principal surface in the base region, a base contact region of the second conductivity type is shallower and has a higher concentration than the base region and is formed between the emitter region and the collector region.

19. A semiconductor device according to claim 16, wherein the concentration of the well region increases continuously from a bottom to a surface.

20. A semiconductor device according claim 16, further

comprising another gate electrode arranged in an opening of the emitter region on a side of the trench.

21. A semiconductor device according to claim 16, wherein the collector region and the well region form an island shape, and the base region exists around the collector and the well regions.

22. A semiconductor device according to claim 16, further comprising an emitter cell and a collector cell arranged alternately lengthwise and crosswise adjacent to each other.

23. A semiconductor device according to claim 16, further comprising at least an emitter contact in an outermost circumference in a group of cells provided in parall el adjacent to each other and that is set larger in size than inner emitter contacts.

24. A semiconductor device according to claim 16, further comprising a base contact region of a second conductivity type having a higher concentration than the base region formed in at least the surface layer portion on the principal surface in the base region in a position, where at least the emitter region in an outermost circumference in a group of cells provided in parallel adjacent to each other is to be arranged.

25. A semiconductor device according to claim 24, wherein

the collector region is surrounded by the emitter region and the base contact region as a planar structure.